Abstract—Comparator is fundamental building blocks in analog-to-digital converters. CMOS comparator which has dual input, dual output inverter stage suitable for high speed analog-to-digital such as flash pipeline ADCs it require high-speed with small chip area low voltage and low power. In this paper a double tail comparator by using clock gating technique is designed in such a way to reduces the overall propagation delay by replacing a existing comparator with a proposed double tail dynamic comparator it reduces the power and voltage by increasing the speed. Without changing the design modified method replace some pair of transistors connected in parallel for proposed comparator due to mismatch in transistor pairs. The design is simulated by using Tanner EDA Tools. The supply voltage (1.2 V) while consuming 9µW in modified comparator. It is shown that in the modified comparator both the power consumption delay time are reduced.

Keywords—Clocked Comparator & High Speed Analog to Digital Converters (ADC), Double Tail Comparator.

I. INTRODUCTION

Comparator is a circuit that it compares two any signals or one analog signal with another signal or any reference voltage and output comes in a binary signal depend on the comparison it works on two phase are reset phase and comparison phase.

Comparators are first developed by the introduction of the dc-coupled amplifier. Comparators is very important building block for many types of circuits including analog-to-digital converters, flash memory, power converters and sensor circuits. Over the years, researchers have been improved the comparator performance in areas, voltage such as sensitivity, offset, speed, and power consumption by using of multistage topologies and other circuit methods[7]. In many applications like e.g., in ADCs knowledge of the signals driving the comparator is used to improve the performance of the comparator and speed.

The basic comparator is a decision-making circuit. If the \((+V_p)\) input is at a greater potential than the \((-V_n)\), then the output of the comparator is a logic 1, whereas if the + input is less potential than the - input then the comparator output is at a logic 0. The basic operational amplifier can be used as a voltage comparator.

A. CLOCKED COMPARATOR

A clocked comparator is a circuit element that makes the decision is that the input signal is low or high at each clock cycle. Regenerative comparators makes the decision fast due to strong positive feedback in the regenerative path[8]. Here we analysising the power and delay of existing comparator, proposed comparator and modified comparator.
There are three stages in this comparator. The pre-amplifier, a positive feedback or decision making stage and an output buffer. The pre-amp stage amplifies the comparator input signal for improving the comparator sensitivity (i.e. by increasing the minimum signal with which the comparator can make a decision fast) and it isolates the comparator input from switching noise which coming from the regenerative feedback stage i.e. kick back noise effect. This effect can be reduced by using Latch based regenerative comparator. The positive feedback stage is mainly used to determine which of the input signals is high or low. The buffer amplifies this information and outputs will be a digital signal. For designing the comparator it first begin by considering input common mode range, power dissipation, propagation delay and comparator gain.

B. CONVENTIONAL DYNAMIC COMPARATOR

The schematic diagram of the conventional dynamic comparator is shown below widely used in many A/D converters consisting high input impedance, rail-to-rail output swing and less static power consumption. The operation of the comparator is as follows it works in two phase.

First is the reset phase when CLK = 0 and Mtail is off, it reset the transistors (M7-M8) and it pulls both output nodes Outn and Outp to VDD it defines a starting condition and it has valid logical level during reset phase. Second is a comparison phase, when CLK = VDD transistors M7 and M8 are off, and Mtail is on. The output voltages (Outp, Outn), are pre-charged to VDD and it start to discharges with different discharging rates Assuming the case when VINP > VINN, then the Outp discharges more faster than Outn, and hence when Outp (discharged by transistor M2 drain current), falls down to VDD before Outn (discharged by transistor M1 drain current), then the corresponding PMOS transistor (M5) will turn on for initiating the latch regeneration speed which is caused by back-to-back regenerative feedback path (M3, M5 and M4, M6). Thus, the Outn pulls to VDD and Outp discharges to ground. If VINP < VINN, the circuits works vice versa.

C. DOUBLE TAIL COMPARATOR

A conventional double-tail comparator is shown in Fig. 5. This comparator topology has less stacking and can operate at lower supply voltages. The double tail enables a large current in the latching stage and wider Mtail2 is a regenerative latching path but it is independent for the input common-mode voltage and a small current in the input stage for low offset [10]. The operation of this comparator is as follows. During reset phase (CLK = 0, Mtail1 and Mtail2 are off) M3-M4 transistors are pre-charged the fn and fp nodes to VDD, which in turn causes MR1 and MR2 transistor to discharge the output nodes to ground signal. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 transistor turn off and voltage at fn and fp nodes starts to drop. The MR1 and MR2 transistor forms the intermediate stage it passes fn node to the cross coupled inverters and it provides a good shielding between input and output signal results in the reduction of kickback noise [7].

The voltage difference at the first stage outputs at time to has an effect on initial differential output voltage and also on the latch delay. Consequently it reduce the delay of the comparator. In this comparator, both intermediate stage transistors will be cut-off finally the fn and fp nodes are discharge to the ground. Besides, during reset phase, these nodes have to be charged from ground to VDD (power
consumption) so it has high peak transient noise at the regeneration time and low kickback noise voltage.

Fig. 5 Schematic Diagram of Double Tail comparator

It has high energy per conversion and input referred as offset voltage than the conventional Dynamic comparator. This Double Tail comparator contains two tail transistors which internally means two current path in it. So, it will increase the performance of the comparator.

II. PROPOSED METHOD

Fig. 6 demonstrates the schematic diagram of the proposed dynamic double-tail comparator. Due to the better performance of this architecture in some of the applications so that the comparator is designed based on the double-tail comparator method[1]. The main idea of this proposed comparator is to increase the regeneration speed by adding two control transistors (Mc1 and Mc2) to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner.

The operation of the proposed comparator is as follows (see Fig. 6). During reset phase CLK = 0, Mtail1 and Mtail2 are off for avoiding static power consumption, M3 and M4 transistor pulls both the fn and fp nodes to VDD and hence Mc1 and Mc2 transistor are in cut off. In intermediate stage the transistors are reset the outputs to ground. During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on) and the transistors M3 and M4 are turn off and in the beginning of reset phase both the control transistors are off. Thus, fn and fp nodes are start to drop with different rates depending on the input voltages. Suppose VND > VNN, then the fn node quickly drops higher than the fp node (since M2 transistor provides more current than M1).

As long as fn node continue to falling then the (Mc1) control transistor it starts to turn on by pulling fp node back to the VDD so that (Mc2) control transistor remains off by allowing fn node to discharged completely. In the proposed structure the comparator detects the node fn discharges faster and a transistor (Mc1) turns on by pulling the node back to the VDD. The difference between fn and fp increases in an exponential manner and latch regeneration time are reduced.

The one important points should be considered in this proposed circuit is when one of the control transistors (Mc1) turns ON then a current from VDD is drawn to the ground via input and the current path transistor (Mtail2) results in static power consumption. To overcome this drawback two NMOS switches are used below the input transistors.

During decision making phase the both fn and fp nodes have been pre-charged to VDD and both switches are closed then fn and fp node start to drop with different discharging rates. As soon as the comparator detects the anyone of the nodes that discharges faster then the control transistors will act as to increase their voltage difference. Suppose the fp node is pulling up to VDD so fn node is discharged completely and
hence the one switch in the charging path of fp node will be opened (in order to prevent any current drawn from $V_{DD}$) but the other switch connected to fn node will be closed to allow the complete discharge of fn node.

### III. MODIFIED COMPARATOR

The operation of the modified conventional comparator is same as proposed comparator instead of adding a clocked gating technique. Gating is a process in a fixed set of condition it permits a second process to occur without any loss. Nowadays, Power has become a main consideration during hardware design and software design. Dynamic power can supply up to 50% of the total power dissipation. Clock Gating most used in design methods to save dynamic and leakage power respectively.

#### IV. SIMULATION RESULT

In order to compare the proposed comparator with the double tail dynamic comparators and modified comparators all circuits have been simulated in a TANNER EDA technology with $V_{dd} = 1.2V$. Fig. 8 shows the waveform of the modified conventional double tail comparator.

#### V. PERFORMANCE ANALYSIS

Comparison table shows the delay over a range of power and supply voltages and as it is shown in the table modified comparator shows minimum Power and Delay.

<table>
<thead>
<tr>
<th>Comparato r structure</th>
<th>Double tail Comparator</th>
<th>Proposed Double Tail Comparator</th>
<th>Double Tail Comparator using Clock Gating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.2v</td>
<td>1.2v</td>
<td>1.2v</td>
</tr>
<tr>
<td>Delay</td>
<td>560pf</td>
<td>398pf</td>
<td>303pf</td>
</tr>
<tr>
<td>Power</td>
<td>12.3µw</td>
<td>11.56µw</td>
<td>9µw</td>
</tr>
</tbody>
</table>
VI. CONCLUSION
In this paper we presented a comprehensive delay analysis for proposed and modified clocked comparators. The common structures of proposed double tail comparator and modified comparator using clock gating shows low power consumption. Also, based on requirements a modified comparator with low voltage low power was proposed in order to improve the performance of the comparator. Simulation results in TANNER EDA technology shows that the delay and power consumption of the proposed comparator is reduced to a great extent in comparison with the existing comparator.

REFERENCES