Characterization of N-Polar GaN Based HEMT Heterostructures for Mixed Signal Applications

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Abstract—GaN-based transistors are attractive for the next-generation RF power and mixed signal electronics due to their high breakdown field and high carrier saturation velocity. III-N high electron mobility transistors (HEMTs) fabricated on the N-face of GaN are well-suited to address the problems of poor electron confinement and high ohmic contact resistance in the highly scaled transistors. At 4 GHz, N-polar metal-insulator-semiconductor (MIS)-HEMTs with a gate length of 0.7 μm exhibited a highest output power density (Pout) of 8.1 W/mm and highest power-added efficiency (PAE) of 71 %, while a Pout of 4.2 W/mm and a PAE of 49% were achieved at 10 GHz. A high speed N-polar MIS-HEMT fabricated with a gate-first self-aligned InGaN-based ohmic contact regrowth technology was characterized, demonstrating an ultra-low contact resistance of 23 n-μm and a state-of-the-art fT•fmax product of 16.8 GHz-μm with a gate length of 130 nm.

Keywords Aluminum Compounds, Gallium Compounds, High-speed Electronics, Microwave FETs, Millimeter Wave FETs, MODFETs, Semiconductor Epitaxial Layers).

I. INTRODUCTION

Much effort has been devoted to establishing the high frequency performance of AlGaN/GaN high electron mobility transistors (HEMTs) over the past decade. The high breakdown field of III-N semiconductors allows AlGaN/GaN HEMTs to operate at much higher voltages than GaAs- or InP-based transistors. Due to the strong spontaneous and piezoelectric polarizations in AlGaN/GaN HEMTs, 2-D electron gas (2DEG) channels with very high charge densities (in excess of 1013 cm-2) can accumulate at the AlGaN/GaN interface. The atomic periodicity of the polarization charges ensures high 2DEG mobilities. These qualities, together with the high density of states and high electron velocity in GaN, make AlGaN/GaN HEMTs an attractive candidate for high frequency electronics in the design of power amplifiers as well as low voltage switching devices.

Most GaN-based HEMTs to-date have been fabricated on the Ga-face (0001) of GaN with little effort devoted to the N-face (0001) orientation. N-polar GaN offers a few unique advantages for highly-scaled GaN-based transistors, providing the opportunity to achieve low ohmic contact resistance in this wide-bandgap semiconductor system and an inherent back-barrier for electron confinement to reduce short channel effects [1]. In this work, we investigated N-polar GaN-based metal-insulator-semiconductor (MIS)-HEMTs as a promising approach to overcome RF power performance bottlenecks encountered in Ga-face AlGaN/GaN HEMTs as their frequency of operation extends into the millimeter-wave and beyond.

We also explored a self-aligned design for N-polar MIS-HEMTs with regrowth of InGaN-based contact layers to simultaneously achieve high cut-off frequencies and high breakdown performance, which are desirable device properties for high speed mixed signal circuits with large voltage swings and wide dynamic ranges.

Fig. 1. Band Diagrams of an undoped and a Si-doped N-Face HEMT. The Si-Doping Prevents the Donor-like Trap State (Er) from being Modulated by the Fermi Level during Transistor Operation.
II. DEVICE DESIGN AND FABRICATION

An N-face HEMT can be simply understood as a Ga-face AlGaN/GaN HEMT turned upside down. Proper engineering of N-face RF devices involve dispersion control not only on the surface (with SixNy passivation) but also within the bulk [2]. Silicon doping was used to eliminate current collapse due to the modulation of trap states near the valence band edge at the AlN/Al(Ga)N interfaces with net negative polarization (Fig. 1). To reduce mobility degradation due to alloy scattering from AlGaN, HEMTs using binary AlN back-barriers or interlayers were adopted.

All devices in this work were grown by plasma-assisted molecular beam epitaxy (MBE) on 6H-SiC substrates. For the design of RF power devices with an AIN back-barrier (Fig. 2) [3, 4], silicon b-doping was used to supply charges to the design of RF power devices with an AIN back-barrier (Fig. 2) [3, 4], silicon b-doping was used to supply charges to the channel and prevent modulation of slow-responding donor-like states near the valence band edge at the bottom AIN/GaN interface. A 3-nm AIN barrier layer induced a 2DEG at the top GaN/AIN interface, above which a 25-nm GaN channel layer was grown. The large conduction band discontinuity of GaN with AIN (ΔE_c), combined with the large dipole moment (ΔEp)_of AIN strained to GaN due to the large polarization coefficients of AIN, enable the use of only a thin layer of AIN to achieve 2DEG confinement potentials larger than the bandgap energy of GaN.

The electrons were further separated from the dopants by a 4-nm GaN-spacer layer to reduce remote ionized impurity scattering. The devices were capped by Al0.1Ga0.9N, which prevented surface degradation during the subsequent high temperature deposition of a 5-nm-thick SixNy gate insulator. A thin cap layer with low AI content (10%) was chosen to minimize depletion of the 2DEG due to its reverse polarization field. To further increase the 2DEG density, a dual-AIN back-barrier scheme was developed using polarization engineering to provide a large total dipole moment, allowing enhanced modulation doping for a higher 2DEG density without parallel conduction.

In highly-scaled designs for millimeter-wave applications, it is necessary to scale the parasitic components along with the gate length. To achieve proper scaling, a gate-first self-aligned MBE InGaN regrowth methodology was developed for fabricating N-polar GaN-based MIS-HEMTs [6]. The device structure consisted of an Al0.3Ga0.7N barrier, an AIN interlayer, and a 10-nm GaN channel with a 5-nm SixNy gate insulator. The resulting 2DEG sheet resistance was 600 nlsq (Fig. 3). A band diagram showing the regrown layer is also shown in Fig. 3.

The graded and n-doped AlGaN kept the Fermi level away from the traps near the valence band edge of the AlGaN/GaN interface [1]. The gate-first process was adapted from the InGaAs MOSFET technology reported by Rodwell et al. and Singisetti et al. [7-8], involving blanket deposition of W/Cr/Sio2/Cr followed by e-beam lithography of gate-fingers using a negative resist and subsequent etching of Cr which acted as a mask for etching the rest of the gate stack. Multiple layers in the gate-stack were chosen to maintain etch-selectivity while etching each layer, with the goal of forming a refractory metal gate capped with SiO2 such that the metals would not be exposed to the MBE chamber during regrowth. SixNy sidewalls deposited by plasma enhanced CVD were formed around the gate by blanket deposition and vertical dry-etch. Graded InGaN layers (40 nm) with an InN cap (10 nm) were regrown in the access regions to achieve a contact resistance (Re) of 23 Ω-um. The schematic of the self-aligned device and a cross-section scanning electron micrograph (SEM) of the regrown area is shown in Fig. 4. Subsequent device fabrication involved height-selective etching of InGaN from the top of the gate to isolate the source and drain [9], followed by deposition of Tibased non-alloyed contacts with LSD = 1 /μm.

III. RESULTS AND DISCUSSION

A. AIN Back-Barrier MIS-HEMTs

Room temperature Hall measurements indicated a 2DEG density and mobility of 7.7x1012 cm-2 and 1350 cm2/Vs, respectively. The maximum drain current Imax was 0.8 A/mm at VG = +2 V. The buffer breakdown at 1 mA/mm, measured between the source and drain of a transistor with the channel etched away, was in excess of 160 V. The two terminal gatedrain breakdown voltage at 1 mA/mm was 48 V. In devices with a gate width of 2x75 μm, an fr of 17 GHz and Imax of 37 GHz were obtained at IDS = 520 mA/mm and VDS = 25 V. Uncooled continuous wave (CW) power measurements were performed at 4 GHz. Biased in deep class AB, measurements at VDS = 35 V and a quiescent drain current density of 100 mA/mm yielded a transducer gain (GT) of 15.3 dB and an output power density (Pout) of 7.1 W/mm with an associated PAE of 58% (Fig. 5). The maximum linear gain was 20 dB in this device. On a separate device, a drain bias of 40 V and a quiescent drain current of 110 mA/mm yielded a GT of 12.7 dB and a high Pout of 8.1 W/mm with an associated PAE of 54% (Fig. 5).
Fig. 3. Large Signal Performance of the AlN Back-Barrier HEMT at 4 GHz with a Drain Bias of (left) 35 V and (right) 40 V. A Highest Pout of 8.1 W/mm was Achieved

B. Self-Aligned MIS-HEMTs with Regrown Ohmic Contacts

Devices with $L_e = 120$ nm showed excellent DC-IV characteristics and transfer characteristics with $I_{\text{max}} = 2.4$ A/mm and peak $g_m = 530$ mS/mm at $V_{DS} = 5$ V, and $I_{D,\text{sat}} = 0.6$ A/mm and $g_m = 350$ mS/mm at $V_{DS} = 500$ mV (Fig. 8). These values were state-of-the-art when compared to the existing GaN/GaN as well as other narrow bandgap systems. As shown in Fig. 9, the extrinsic $g_m$ remained relatively flat with increasing $I_D$, indicating that the $g_m$-dropoff due to a source choke was effectively eliminated by a self-aligned structure. Due to the self-aligned nature of the devices, no DC-RF dispersion was observed (Fig. 9). The two-terminal breakdown voltage at $I_{\text{max}}/A/mm$ for a 250-nm gate-length device was 10 V, while the destructive breakdown voltage was at 25V.

Fig. 4. (Left) DC-IV characteristics of a self aligned transistor with $L_e = 120$ nm showing a record high $I_{D,\text{sat}}$ of 2.4 A/mm and low onresistance of 600 nΩ/mm for $(V_{gs}-V_{T}) = 7$ V. (Right) Transfer characteristics showing a peak $g_m$ of 350 mS/mm at $V_{OS} = 500$ mV

Imax of 17.5 GHz for $L_e = 120$ nm. $R_g$ and $C_{gd}$ values were extracted to be 1400 nΩ and 0.1 pF/mm, respectively. The large value of $R_g$, attributed to a thin gate stack (100 nm) of W/Cr, could be the main cause of low $I_{\text{max}}$. Simulating the same circuit with $R_g = 5$ nΩ yielded an $I_{\text{max}}$ value of 250 GHz, thereby confirming the hypothesis. Self-aligned T-gate technology was therefore developed and tested on devices with $L_e = 111$ nm, resulting in $I_{\text{max}}$ of 10 GHz and $I_{\text{max}}$ of 21 GHz at $V_{DS} = 4$ V. These values were similar to those of non-selfaligned devices at a similar drain bias. Fabrication of submicron devices with the T-gate process is ongoing. As shown in Fig. 10, the total delay ($t_{\text{total}}$) scaled linearly with $L_e$ indicating that the effect of the parasitic components has been minimized in a self-aligned structure. These devices showed a state-of-the-art $t_{\text{total}}$ product of 16.8 GHz-$A/mm$ and exceptional performance at low supply voltages ($V_{DS} = 500$ mV), thereby making GaN competitive to not only wide bandgap materials such as SiC but also narrow bandgap technologies such as InGaAs and InSb by offering both low knee voltages and high drive currents while maintaining relatively high breakdown voltages for unipolar (non-CMOS like) operation [10].

Fig. 5. (Left) Total delay ($t_{\text{total}}$) versus $L_e$ for self-aligned HEMTs showing linear scaling with minimal effect of parasitic components. (Right) Comparison of our best self-aligned device with state-of-the-art GaN technology highlighting effective delay reduction with a self-aligned structure

IV. CONCLUSION

We demonstrated N-polar GaN-based MIS-HEMTs with decent microwave power performance in the C- and X-bands, as well as self-aligned fabrication of N-polar transistors with excellent output characteristics and effective scaling of parasitics. By combining the high speed and high breakdown properties of GaN-based heterostructures with back-barrier engineering and self-aligned processes using N-polar GaN for further scaling, GaN HEMTs can be made useful for low voltage mixed signal applications which is an area that has not been explored for III-N electronics to a large extent so far.
REFERENCES


